データ駆動プロセッサの研究経緯

'82 '83 '84 '85 '86 '87 '88 '89 '90 '91 '92 '93 '94 '95 '96 '97 '98 '99 2000 '01 '02 '03 '04 '05 '06 '07 '08 '09 '10 '11

Feasibility Study

Q-p

TTL Version

(2~4MOPS)

Q-v1

Multi Chip Version

(20MOPS)

Q-x

Single Chip Version

(40MOPS)

Video Signal Processing Oriented

DDP / TAM

4PE Super-Integration

(600MOPS)

CUE Project

CUE-p

8PE (2.9GOPS)

CUE-v1

12PE (4.7GOPS)

CUE-v2

3PE (9.6Gbps)

CUE-v3

4PE

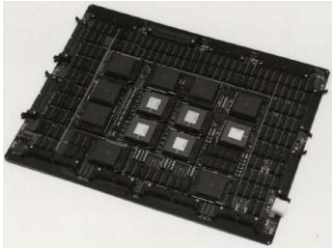
(CUE-v2 based)

ULP-DDCMP

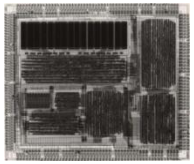
4PE(ULP-CUE)

MOPS: Mega Operation Per Second
GOPS: Giga Operation Per Second
Gbps: Giga bit per second

Q-p

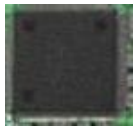


Q-v1



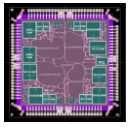
Q-x
1.3um

CUE-p
0.35um

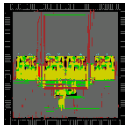


CUE-v1
0.25um

CUE-v2
0.18um



CUE-v3
90nm



ULP-DDCMP
65nm